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|---|---|
| CHU, GABRIEL L | |
| **ART UNIT** | **PAPER NUMBER** |
| 2184 | 13 |

DATE MAILED: 10/27/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/394,302 | DEAN ET AL. | |
| | Examiner | Art Unit | |
| | Gabriel L. Chu | 2184 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *17 September 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *55-70 and 84-96* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *55-70 and 84-96* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 84-85, 87-89, 91-92, and 94-95 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6452411 to Miller et al. Referring to claim 84, Miller et al. disclose an integrated circuit chip test device adapted to test integrated circuit chips, said device comprising: a test board (See figure 1.); sockets on said test board, said sockets being adapted to hold integrated circuit chips to be tested (From line 47 of column 3, "Coupling the DUTs to the channel is the interface circuitry 116.); and testing circuitry on said test board electrically connected to said sockets, wherein said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets, such that said testing circuitry tests all of said integrated circuit chips simultaneously, and wherein said testing circuitry identifies a defective integrated circuit chip as one having a different output when compared to outputs of the other integrated circuit chips, when all said integrated circuit chips are supplied with identical inputs (From the abstract, "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the

known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from the abstract, "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD." Further, from the technical field, "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel." Wherein a faulty circuit's output is different.).

Referring to claims 85 and 92, Miller et al. disclose all of said integrated circuit chips have an identical design (From line 6 of column 3, "As briefly summarized above, an embodiment of the invention provides for more efficient testing of a number of similar, and preferably identical, IC devices in parallel without altering the test program or the conventional tester.").

Referring to claims 87 and 94, Miller et al. disclose a memory attached to said test board, said memory being adapted to store test results (From line 54 of column 4, "Each comparator 224 generates raw error data being the result of bit-wise XOR operations performed upon a DUT data value and a KGD data value. This raw error data may be stored either in the CSRs 220, or in a memory (not shown) separate from each block 120.sub.i. The tester 104 may then access this memory at a later time, through the channel 108 or through an alternative path, to read the raw error data.").

Referring to claim 88, Miller et al. disclose known good integrated circuit chip

attached to said board (From the abstract, "A system for testing integrated circuit devices is disclosed in which a tester communicates with a known good device through a channel.").

Referring to claims 89 and 95, Miller et al. disclose all of said comparators are connected to said known good integrated circuit chip such that any integrated circuit chips that produce an output different than the output produced by said known good integrated circuit chip is identified as a defective integrated circuit chip (From the abstract, "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs). The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD.").

Referring to claim 91, Miller et al. disclose an integrated circuit chip test device adapted to test integrated circuit chips, said device comprising: a test board (See figure 1.); sockets on said test board, said sockets being adapted to hold integrated circuit chips to be tested (From line 47 of column 3, "Coupling the DUTs to the channel is the interface circuitry 116.); testing circuitry on said test board electrically connected to said sockets (See figure 1, 104.); and a golden socket for a known good integrated circuit chip (See figure 1, 112 and its connecting means.), wherein said testing circuitry includes comparators arranged in parallel and electrically connected to said sockets,

such that said testing circuitry tests all of said integrated circuit chips simultaneously, and wherein said testing circuitry identifies a defective integrated circuit chip as one having a different output when compared to outputs of the other integrated circuit chips and the output of said known good integrated circuit chip, when all said integrated circuit chips and said known good integrated circuit chip are supplied with identical inputs (From the abstract, "Tester-DUT interface circuitry is provided for monitoring the channel while the tester is writing data as part of a test sequence to locations in the known good device. In response, the interface circuitry writes the data to corresponding locations in each of a number of devices under test (DUTs)." Further, from the abstract, "The interface circuitry monitors the channel while the tester is reading from the locations in the known good device (KGD), and in response performs a comparison between DUT data read from the corresponding locations in the DUTs and expected responses obtained form the KGD." Further, from the technical field, "This invention is related to the testing of integrated circuit devices using a semiconductor tester, and more particularly to testing a number of devices in parallel." Wherein a faulty circuit's output is different.).

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 55-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 4291404 to Steiner in view of US 6452411 to Miller et al. Examiner maintains the rejection which can be found in paper no. 11.

5. Claim 70 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 4291404 to Steiner in view of US 6452411 to Miller et al. as applied to claim 63 above, and further in view of US 6499121 to Roy et al. Examiner maintains the rejection which can be found in paper no. 11.

6. Claims 86 and 93 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6452411 to Miller et al. as applied to claims 84 and 91 above. Referring to claims 86 and 93, although Miller et al. do not specifically disclose visual test failure indicators attached to said test board, such that one of said visual test failure indicators is adjacent each of said sockets, individual indicators are notoriously well known in the art. Examiner takes official notice for having individual indicators. A person of ordinary skill in the art at the time of the invention would have been motivated to use individual indicators in a testing system testing multiple devices because it provides immediate information regarding a particular device.

7. Claims 90 and 96 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6452411 to Miller et al. as applied to claims 84 and 91 above, and further in view of US 6499121 to Roy et al. Referring to claims 90 and 96, although Miller et al. does not specifically disclose by comparing whether outputs of all integrated circuit chips are identical, said testing circuitry does not require a specific proper output that a given input should produce for the specific design of the integrated circuit chip being

tested, testing without a known output is known in the art. An example of this is given by Roy et al. in line 13 of column 2, "Accordingly, an embodiment of the invention is directed to interface circuitry that essentially acts as a relay between the tester and a number of DUTs, where test vectors on each channel are fanned out to multiple DUTs. In general, the test vectors include stimuli, such as addresses, data values, and control signals, that are passed on to the DUTs while maintaining any timing constraints between the stimuli that were set up by the tester. The responses by the DUTs to these stimuli may then be collected by the interface circuitry and relayed back to the tester. If desired, the interface circuitry may be further enhanced with error detection capability based on the responses. For instance, the response from each DUT may be evaluated for internal consistency, by within-DUT and across-DUT comparisons, or it may be evaluated by comparison to expected responses received from the tester. The results of the comparison may then be provided back to the tester in summary or in detail form." Further, from line 55 of column 6, "The interface circuitry 226 responds in step 620 by reading from its corresponding DUTs, and performs comparisons of data values across DUTs and/or within DUTs to determine any errors in the DUTs. For instance, the interface circuitry 226 may be configured to perform comparisons of groups of bits read from locations within the same DUT, where each group had the same bit pattern written to them in step 618. Such a conventional technique is discussed below in connection with FIG. 7. In addition or instead of the conventional technique, the interface circuitry 226 can be further configured to perform comparisons of bits read from locations in different DUTs. This latter technique is described below in relation to

FIG. 8. A combination of these two techniques of "within word" and "across DUT" comparisons is illustrated in FIGS. 9a and 9b. Thus, in contrast to the embodiment of FIG. 5, the tester 108 in FIG. 6 does not send expected data to the interface circuitry 226 during the test sequence. Rather, the interface circuitry 226 performs cross-DUT and within-DUT comparisons, such as in FIGS. 7-9 below, and optional statistics, to predict errors in the DUTs with relatively high confidence. Appropriate storage of the error data and compression also takes place. Eliminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology." A person of ordinary skill in the art at the time of the invention would have been motivated to incorporate the teachings of Roy et al. into a circuit tester because, from line 8 of column 7, it "predict[s] errors in the DUTs with relatively high confidence", and further from line 10 of column 7, "[e]liminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology."

***Response to Arguments***

8. Applicant's arguments filed 17 September 2003 have been fully considered but they are not persuasive. Examiner views the Applicant's invention, in claims 55-70, as a combination of two concepts, testing and portability. From the rejection, the testing concepts claimed are known in the art, and portable circuit testing is known in the art. While, in the rejection for claims 55-70, a portable tester for testing multiple ICs was not presented, the testing of multiple ICs was presented, such testing comprising the testing concepts presented by Applicant. From the remarks presented in paper no. 12, it

appears that Applicant is arguing that the invention is therefore patentable over the prior art because Applicant has made a circuit tester, of known functionality, portable.

In response to Applicant's remark on page 7 (with emphasis), "Steiner... does not disclose any form of an in-transit test box for holding test board**s**", Examiner acknowledges a typo in line 5 of the first paragraph of the rejection of claims 55-69 of the office action of paper no. 11. However, it should be clear that the intended word was "board", singular, and not "boards", plural. Evidence of this is shown in "a test board" of the previous line of the same action, "said test board" of the following line of the same action, and "Although Steiner does not specifically disclose a plurality of test boards" of the following sentence of the same action.

In response to Applicant's remark on page 9 that "neither Miller nor Steiner describes testing circuitry that operates while in transit", Examiner interprets this as tested in the portable circuit tester. Referring to claims 55 and 63, Applicant specifically claims, "tested while being transported". Applicant makes no claim as to the degree or nature of such transportation, or to the relativity of motion, therefore a circuit that is placed in a portable circuit tester is deemed to be in transit.

9. In response to applicant's argument that the multiple circuit tester of Miller et al. is not combinable with the portable circuit tester of Steiner, and further, the combination of Roy et al. with Steiner in view of Miller et al., the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of

the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, Examiner is applying the multiple circuit testing functionality of Miller et al. to the portable circuit testing idea of Steiner. A person of ordinary skill in the art would have been motivated to test more than one integrated circuit on a plurality of receptacles because, from line 4 of column 2 of Miller et al., it "increase[s] the throughput of the test system in terms of the number of DUTs tested per unit time". Further, a person of ordinary skill in the art at the time of the invention would have been motivated to render a device portable because, from line 7 of column 2 of Steiner, it "allows use of the device in the field." Further, a person of ordinary skill in the art at the time of the invention would have been motivated to incorporate the teachings of Roy et al. into a portable circuit tester because, from line 8 of column 7 of Roy et al., it "predict[s] errors in the DUTs with relatively high confidence", and further from line 10 of column 7 of Roy et al., "[e]liminating the cycle of sending expected data may further reduce the time needed to test the DUTs, thus promoting a more efficient testing methodology." Other examples of the application of portability to a device include such items as computers (laptops), clocks (watches), phones (cordless and wireless), radios (such as car stereos or a "Walkman"), and DC-to-AC converters.

***Conclusion***

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays with alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

gc

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